REMARKS

Claims 1-21, 23 and 27-33 are pending in the present application. Claim 22 was previously canceled, and claims 24-26 are canceled herein. Claim 1 has been amended. No new matter has been added. Applicant respectfully requests reconsideration of the claims in view of the following remarks.

Claims 1-11, 18, 19, 23-25 and 27-31 have been rejected under 35 U.S.C. § 103(a) as assertedly being unpatentable over U.S. Patent No. 2004/0094820 to Nishikawa, *et al.* (hereinafter "Nishikawa"). Claims 12-17, 20, 21, 26 and 31-32 have been rejected under 35 U.S.C. § 103(a) as assertedly being unpatentable over Nishikawa in view of U.S. Patent No. 5,758,100 to Odisho, *et al.* (hereinafter "Odisho").

Claim 1, as amended, requires that:

> in an external access operating mode of the second semiconductor device, the voltage supply device of said second semiconductor device provides the supply voltage for the second semiconductor device, and, in a standby or refresh operating mode of the second semiconductor device, the voltage supply device of said first semiconductor device provides the supply voltage for the second semiconductor device.

The Nishikawa reference does not teach or suggest external access, standby, refresh or any other operating modes of a first or second semiconductor device. Instead, the components (e.g. 201e-209e) in Nishikawa operate in either a first delay path or a second delay path and/or at voltage level VDD1 or VDD2. Nishikawa at [0095]-[0096]. Moreover, there is no teaching or suggestion in Nishikawa that the selection of voltage level VDD1 or VDD2 is dependent upon an operating mode of the components. Instead, some components, such as 207e-209e, may use either voltage level without regard to and independently of operating mode or delay path. Nishikawa at [0096].

Odisho also fails to teach or suggest that an external access, standby, refresh or any other operating mode of a first or second semiconductor device affects the selection of a voltage supply device for that semiconductor device. Instead, Odisho merely discloses a memory 108 that can be accessed by a processor 104. Col. 2, lns. 18-21. Odisho provides no teaching regarding the operating modes or power supply of memory 108 or any other semiconductor device. In the final Office Action, in the section addressing canceled claim 26 at pages 8-9, the Examiner appears to interpret "external access" as requiring physical access. Applicant traverses this interpretation and submits that it is clear from the disclosure of the present application that the claimed external access is an electrical access.

In view of the above, Applicant respectfully submits that this response complies with 37 C.F.R. § 1.116. Applicant further submits that the claims are in condition for allowance. No new matter has been added by this amendment. If the Examiner should have any questions, please contact Applicant's attorney at the number listed below. No fee is believed due in connection with this filing. However, in the event that there are any fees due, please charge the same, or credit any overpayment, to Deposit Account No. 50-1065.

Respectfully submitted,

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Date

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